IMS 2017 5G Summit: RFIC/CMOS Technologies for 5G, mmW and Beyond

Ali M. Niknejad
Berkeley Wireless Research Center
BWRC xG Vision (x >= 5)

Mesh Backbone

xG Hub "eWall"

Class B

Class A, C

Class D

1km

500m

5m

10m
Stay Wireless

- In Europe, ~50% of LTE base stations are wireless. Why not use the same technology for front- and back-haul
Interference Mitigation

- Maxwell’s equations are linear: waves just pass through each other.
- Interference really happens because of the receiver’s non-linearity.
- Most radios today spray energy in all possible directions.
- This is not only a huge waste of power, but it causes more interference!
- Solution: directivity!
TECHNOLOGY TRENDS
CMOS Raw Speed

CMOS Fmax is not getting better
... but power lower for a given frequency ...
High speed analog / mixed-signal improves
**Receiver Sensitivity**

\[ F_{\text{min}} > 1 + 2 \left( \frac{f}{f_T} \right) \sqrt{\frac{\gamma}{\alpha}} \frac{1}{5} \]

- Receiver will have a noise figure \( \sim 3 \text{ dB} \) higher than \( \text{Nfmin} \) of device
- 28 nm: 4-5 dB NF at 100 GHz
Silicon Power Amplifier Performance

- Obvious trends: Power and Efficiency drop with frequency.
- Power can be improved by on-chip and spatial combining.
- Going beyond 17 dBm with CMOS difficult and inefficient
  - With modest array (64 elements), don’t need much more power
  - Handset is key issue that would benefit from III-V (e.g. GaN)
Typical mm-Wave Class-A PA Power/Efficiency Characteristics

Psat

P1dB 15%

6dB BO 8%

2%
# Phase Noise

<table>
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<tr>
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<tbody>
<tr>
<td></td>
<td>40nm</td>
<td>90nm</td>
<td>130nm</td>
<td>40nm</td>
<td>65nm</td>
<td>32nm SOI</td>
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<table>
<thead>
<tr>
<th>Type</th>
<th>Harmonic extraction</th>
<th>Fundamental</th>
<th>Fundamental</th>
<th>Fundamental</th>
<th>Frequency tripling</th>
<th>Common-mode extraction</th>
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<tbody>
<tr>
<td>Quadrature output</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
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<table>
<thead>
<tr>
<th>$P_{DC}$ (mW)</th>
<th>Oscillator</th>
<th>Buffer</th>
<th></th>
<th></th>
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<tbody>
<tr>
<td></td>
<td>13.5</td>
<td>10.5</td>
<td>14</td>
<td>3.9</td>
<td>30</td>
<td>10.6+14(a)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NA</td>
<td>NA</td>
<td></td>
<td></td>
<td>35</td>
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</tbody>
</table>

| Supply voltage (V) |                      |             |            |            |                    |                        |
|                    | 0.7/1                | 1.2         | 1          | 0.9        | 1.2                | 1                      |

| Tuning range (GHz) |                      |             |            |            |                    |                        |
|                    | 48.4-62.5 (25.4%)    | 55.8-61.6 (9.75%) | 59-65.2 (10%) | 57.9-68.3 (16.2%) | 58.3-65.4 (11.5%) | 46.4-58.1 (22.4%) |

<table>
<thead>
<tr>
<th>Phase noise (dBc/Hz)</th>
<th>1MHz</th>
<th>10MHz</th>
<th>1MHz</th>
<th>10MHz</th>
<th>1MHz</th>
<th>10MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-100.1</td>
<td>-122.3</td>
<td>181.5</td>
<td>183.7</td>
<td>189.6</td>
<td>191.8</td>
</tr>
<tr>
<td></td>
<td>-94</td>
<td>NA</td>
<td>177.7</td>
<td>NA</td>
<td>177.9</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td>-95 / -91(e)</td>
<td>NA</td>
<td>185 / 181</td>
<td>NA</td>
<td>185 / 181</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td>-92.5</td>
<td>NA</td>
<td>173.1</td>
<td>NA</td>
<td>177.3</td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td>NA</td>
<td>-115(b)</td>
<td>NA</td>
<td>-115(b)</td>
<td>NA</td>
<td>-118(b)</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>$F_{oM}$ (dBc/Hz)</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1MHz</td>
<td>185 / 181</td>
<td>173.1</td>
<td>NA</td>
<td>168.5</td>
<td>176.9</td>
<td>177.5</td>
</tr>
<tr>
<td>10MHz</td>
<td>185 / 181</td>
<td>187.3</td>
<td>NA</td>
<td>175.5</td>
<td>178.1</td>
<td>184.5</td>
</tr>
</tbody>
</table>

[Courtesy of Masoud Babaie]
ADC Resolution (ENOB)
ADC Power

- 2 GS/s, 8-bits @ 100fJ/conv $\rightarrow$ 50mW
- Clock jitter requirements (0.5 ps), ADC buffer (especially SAR), reference buffer …
Technology Trends Summary

- Operation up to 100 GHz possible with CMOS / SiGe
- Receiver noise figure not an issue
  - Especially in an array
- Phase noise is dominated by reference noise
  - 64-QAM at 1 Gb/s at 28 GHz possible
- Tx efficiency a major issue
  - < 5% with current techniques at 6-dB back-off
  - Composite signals (multiple streams) may require 10-dB backoff!
- ADCs getting better … especially moderate resolution @ 1 Gb/s (4-6 bits)
MASSIVE MIMO AND MM-WAVE SYSTEM ARCHITECTURE
BWRC Past mm-Wave Chips

[Tabesh et al, ISSCC 2011]

4 Elements (Separate TX/RX)
137 mW Total (Rx or Tx mode)

[Tabesh et al, VLSI/JSSC 2015]
24/60 GHz RFID; 12 Mbps; 1.5 uW

[Chen et al, ISSCC 2011]
18.6dBm 60GHz Power Amplifier in 65nm

[Chen et al, ISSCC 2013]
Peak Tx efficiency 17.4%. Maintains > 7% efficiency while transmitting 6 Gbps (16-QAM)
MIMO vs. Beamforming

- A fully digital MIMO allows us to trade-off spatial diversity of channel in various ways
  - Higher capacity through multiple streams
  - Beam forming, Multi-user beam forming
  - Spatial diversity
  - But MIMO requires ADC/DAC per element

- Analog/RF beamforming requires only phase shifters, which can be done in the analog / RF domain → lower power transceivers, arguably reduced performance requirements from analog/baseband blocks (ADC)
  - Grating lobes can be reduced with tapering
  - Time-division multiple beam access for multi-user

- A hybrid solution is desirable
  - Long range beams, short range multi-beams …
Massive MIMO

- A very large number of antennas, much larger than the number of user beams; form “beams” from the basestation to users simultaneously
- Computation of channel matrix simplified in TDD systems if we invoke reciprocity. FDD is problematic

Can choose beamforming coefficients either using beam forming (peak gain in the direction of desired user) or Zero Forcing (ZF) – nulls in the direction of other users, which reduces gain but improves multi-user capacity
State-of-Art Massive MIMO

- 128 antennas
- 20 MHz of channel bandwidth
- 125 Gbit/s aggregated into central baseband DSP engine

What happens when we need 100x more throughput??

Need less of a “brute force” architecture
BWRC’s Hydra: Massive mm-Wave MIMO

- Many more elements at base station than users ($M \gg K$)
- Users are simple and ignorant of channel matrix
- FE circuitry has relaxed noise performance due to array averaging
- Multipliers in BF also have relaxed noise performance
First Prototype Receiver (Sim)

<table>
<thead>
<tr>
<th>f0</th>
<th>75 GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>BW,BB</td>
<td>2 GHz</td>
</tr>
<tr>
<td>AC Gain</td>
<td>21-22dB</td>
</tr>
<tr>
<td>NF</td>
<td>8-10 dB</td>
</tr>
<tr>
<td>Input P1dB</td>
<td>-18 dBm</td>
</tr>
<tr>
<td>Pdc</td>
<td>8 mW</td>
</tr>
<tr>
<td>Area</td>
<td>200x450um²</td>
</tr>
</tbody>
</table>

- Goal is low power per channel
- Mixer first receiver; IF multi-user phase shifting
- Trade-off noise but don’t give up linearity

Tech: CMOS 28nm
xG “Array” Publications

Design of Energy- and Cost-Efficient Massive MIMO Arrays

This paper discusses how multiuser massive microwave and mm-wave MIMO can support communications among many users over a given allocation of spectrum, along with manageable array form factors and power consumption.


“THz” Communication

We demonstrated 240 GHz with 16 Gbps (65nm)
- On-chip antennas
- QPSK: Modulate at 80 GHz → Tripler
  - 14 pJ/bit Tx + 16 pJ/bit Rx
  - Up to 1 meter range with dielectric lenses

Can we improve energy efficiency with technology scaling?

Highest achievable data rate / energy efficiency?
- More complex modulation schemes?

[Thyagarajan, Kang, Niknejad, RFIC 2014]
Conclusion

- Massive MIMO:
  - Beam forming, beam nulling
  - 10X higher spatial capacity

- Mesh networking and wireless backhaul

- mm-Wave
  - 10 GHz → 100 GHz for up to 1 km
  - > 100 GHz for shorter ranges

- Design the entire array, not individual blocks
  - PA output power reduced per element
  - Receiver noise figure can trade-off with array
  - Need to carefully consider phase noise / coherence across array
Acknowledgements

- Collaborators: Elad Alon, Bora Nikolic

- Our research vision comes from years of research funded by NSF, DARPA, the UC Discovery Program, and our industrial sponsors at BWRC

  - DARPA TEAM program (60 GHz)
  - DARPA Wafer Scale Radio Seedling
  - DARPA RF-FPGA Program
  - UC Discovery Program:
    - CMOS “Digital” Transmitters
    - FCRP-C2S2 Program

- And many continuing programs!
  - NSF EARS

- And of course industry collaborations.